

ABSTRACT

A non-volatile memory circuit comprising first and second transistors (101, 102) each having a gate and a drain, wherein the gates of these transistors are connected to each other and the drains of these transistors are connected to each other, whereby a first inverter is formed; third and fourth transistors (103, 104) each having a gate and a drain, wherein the gates of these transistors are connected to each other and the drains of these transistors are connected to each other, whereby a second inverter is formed; a fifth transistor (105) provided with a gate, which is connected to a word line (107), and which is connected between a first bit line (108) and an input terminal of the second inverter; a sixth transistor (106) provided with a gate, which is connected to the word line (107), and which is connected between a second bit line (109) and an input terminal of the first inverter; and first and second resistor elements (114, 115) which are serially connected to the first and second inverters, respectively, wherein the input terminal and an output terminal of the first inverter are connected to an output terminal and the input terminal of the second inverter, respectively, and the resistance values of the first and second resistor

elements (114, 115), which are connected to a ground line (111), are electrically variable.